2188

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To Whom It May Concern:

Enclosed please find document listed below that was mailed to our firm which does not appear to belong to us.

09/741494 Three Months Office Action Applicant Kendell A. Chilton

Thank you,

Tina Han
U.S. Docketing Agent
Knobbe, Martens, Olson & Bear LLP.
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Office Action Summary

Application No.	Applicant(s)	
09/741,494	CHILTON, KENDELL A.	
Examiner	**Art Unit**	
Reginald G. Bragdon	2188	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 December 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings filed on 19 December 2000 have been approved by the Examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 20, it is not clear where Applicant has set forth in the specification that the status includes "a non-reserved value as a tag indicator when the data element is valid" or " a reserved value as the tag indicator when the data is invalid".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 11-14, 21-24, and 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Walton et al. (6,389,494; supported by the incorporated reference Walton, 6,145,042).

As per claims 1, 11, and 21, Walton et al. ('494) teaches a data storage system including a host computer 112, disk drive bank 116, and interface 118. The interface includes cache memories 120. See figure 2. A DRAM cache memory (e.g. cache memory 0; "volatile cache memory") is connected to the director (e.g. front end director 0) through a point-to-point serial bus 126 (e.g. serial bus $126_{0,1}$). See column 4, lines 1-3. Walton et al. ('494) further indicates that a description of control/data bus requests and effecting the transfer in response to a control/data bus grant is in accordance with a protocol, using the ASICs of the cache memory (see figure 3), described in co-pending application 08/996,809 (now U.S. Patent 6,145,042 to Walton), which is incorporated by reference in Walton et al. ('494).

Walton ('042) teaches a asserting a command including a read or write operation request and an address ("providing a command") from a controller. See column 6, lines 37-48. Data is written to or read from the cache memory ("moving a data element"). See column 6, lines 37-48. Upon the end of the write operation, an end status signal is reported ("receiving status...in accordance with the data element"). See column 6, lines 55-58. The controller of Walton ('042) is equivalent to one of the directors of Walton et al. ('494). The controller of Walton et al. ('494) is connected to the cache memory over a point-to-point connection, and therefore all transactions between a director and a cache memory occur over the point-to-point connection.

As per claim 30, the claim is rejected for the reasons set forth with respect to claim 1, above. Furthermore, with reference to figure 4, Walton et al. ('494) teaches a front-end director including bus interfaces connected to a host computer (each bus adaptor represents a "first adaptor"), a crossbar switch 123 connected to the point-to-point connections, and a CPU ("controller").

As per claim 31, the claim is rejected for the reasons set forth with respect to claim 1, above. Furthermore, with reference to figures 3 and 6, Walton et al. ('494) teaches a coupling node 130 ("adaptor"), memory regions A-D ("memory locations"), and a plurality of ASIC (each representing a "controller").

As per claims 2-4, 12-14, and 22-24, Walton et al. ('494) teaches that each serial bus 126 is a 4-wire bus having a differential pair of receive wires and a differential pair of transmit wires. See column 4, lines 3-6. The receive and transmit wires are unidirectional wires. All information passing from a director to a cache memory would pass through one set of wires (e.g. a command through the transmit wires) and all information passing from a cache memory to a director (e.g. status) would pass through the other set of wires (e.g. receive wires).

6. Claims 1, 11, 21, and 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimoto et al. (6,578,108).

As per claims 1, 11, and 21, Fujimoto et al. teaches, with reference to figure 1, a selector 13 ("interface circuit") connected via a point-to-point access path 136 to a cache memory 14. Figure 7 shows the interactions between the selector unit and the CM controller located within the cache memory 14 (see figure 6). As shown in figure 7, a REQ 506 is sent from the selector unit to the CM controller ("providing a command"). Data 509 is also sent from the selector unit

to the CM controller ("moving a data element"). Finally, status information 513 is sent from the CM controller to the selector unit ("receiving status").

As per claim 30, the claim is rejected for the reasons set forth for claim 1, above. Fujimoto et al. further teaches, with reference to figure 5 and the corresponding description at column 8, line 53, to column 9, line 20, the selector unit 13 which includes a path IF 301 connected to the host device through the CM controllers ("first adaptor"), a path IF 301 connected to the cache 14 ("second adaptor"), and a data transfer control unit 315 ("controller").

As per claim 31, the claim is rejected for the reasons set forth for claim 1, above. Fujimoto et al. further teaches, with reference to figure 6 and the corresponding description at column 9, lines 21-48, the cache memory unit 14 connected to the selector unit through path IF 301 ("adaptor"), memory modules 106 ("memory locations"), and data transfer controller 315.

7. Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Steinmetz et al. (6,425,034).

As per claims 1, 11, and 21, Steinmetz et al. teaches a fibre channel system including a host bus adapter 182 (figure 4; "interface") connected through a fibre channel FC 188 to a disk array controller 200 (figure 6; "volatile cache memory circuit") which includes a cache memory 210. The FC 188 represents a point-to-point channel between the host bus adaptor and the disk array controller. Shown in figures 3A and 3B are the read and write process between an initiator and target using the fibre channel protocol. An initiator (e.g. host through host bus adapter 182) sends a command to the target (e.g. cache of disk array controller 200). Data is transmitted between the initiator and target, the direction of data transmission depending upon whether the

operation is a read or a write. Finally, status information is returned via a FCP_RSP sequence. See column 7, line 59, to column 8, line 16.

As per claims 2-4, 12-14, and 22-24, the fibre channel protocol includes unidirectional links as shown in figure 1B. All information passing from the host adapter to the disk array controller would pass through one set of wires (e.g. a command through the transmit wires) and all information passing from the disk array controller to the host adapter (e.g. status) would pass through the other set of wires (e.g. receive wires).

As per claims 5, 15, and 25, Steinmetz et al. teaches that the fibre channel protocol transmits data in units of frames. As shown in figure 2, the frames (for both reads and writes) include synchronization delimiters, such as "start-of-frame" and "end-of-frame".

As per claims 6, 16, and 26, Steinmetz et al. teaches that the fibre channel protocol transmits data in units of frames. As shown in figure 2, the frames (for both read and writes) includes CRC error check information.

As per claims 7, 17, and 27, Steinmetz et al. teaches read and write transactions as detailed above. Steinmetz et al. further teaches encoding the frames using the 8B/10B encoding/decoding scheme. See column 33, lines 20-38.

As per claims 8, 18, and 28, Steinmetz et al. teaches a busy signal at column 30, lines 1-2.

As per claims 9, 19, and 29, Steinmetz et al. teaches sending a frame header including an exchange identifier ("tag"). See column 6, lines 58-62.

As per claims 10 and 20, Steinmetz et al. teaches partitioning the sequence of read data if the data is larger than a frame. See column 7, lines 65-67. The multiple frames would be recombined at the host adapter ("processing the read data element").

As per claim 30, the claim is rejected for the reasons set forth above for claim 1. Furthermore, with reference to figure 22, Steinmetz et al. teaches the fibre channel controller which includes a host system interface ("first adapter"), inbound frame buffer unit ("second adapter"), and an inbound sequence & exchange management unit ("controller").

As per claim 31, the claim is rejected for the reasons set forth above for claim 1. Furthermore, with respect to figure 6, Steinmetz et al. teaches an FC controller 206 ("adapter"), cache memory 210 ("memory locations"), and a microprocessor ("controller").

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Walton (5,943,287) is incorporated by reference in the Walton et al. ('494) reference.

Sne et al. (5,890,207) teaches a cached disk array.

9. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
September 25, 2003